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# **Atomically Precise Graphene Nanoribbon** Transistors with Long-Term Stability and Reliability

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Supporting Information

**ABSTRACT:** Atomically precise graphene nanoribbons (GNRs) synthesized from the bottom-up exhibit promising electronic properties for high-performance field-effect transistors (FETs). The feasibility of fabricating FETs with GNRs (GNRFETs) has been demonstrated, with ongoing efforts aimed at further improving their performance. However, their long-term stability and reliability remain unexplored, which is as important as their performance for practical applications. In this work, we fabricated short-channel FETs with nine-atomwide armchair GNRs (9-AGNRFETs). We revealed that the onstate  $(I_{ON})$  current performance of the 9-AGNRFETs deteriorates significantly over consecutive full transistor on and off

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logic cycles, which has neither been demonstrated nor previously considered. To address this issue, we deposited a thin  $\sim 10$ nm thick atomic layer deposition (ALD) layer of aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) directly on these devices. The integrity, compatibility, electrical performance, stability, and reliability, of the GNRFETs before and/or after Al<sub>2</sub>O<sub>3</sub> deposition were comprehensively studied. The results indicate that the observed decline in electrical device performance is most likely due to the degradation of contact resistance over multiple measurement cycles. We successfully demonstrated that the devices with the Al<sub>2</sub>O<sub>3</sub> layer operate well up to several thousand continuous full cycles without any degradation. Our study offers valuable insights into the stability and reliability of GNR transistors, which could facilitate their large-scale integration into practical applications.

**KEYWORDS:** nanoelectronics, graphene nanoribbons (GNRs), two-dimensional (2D) materials, semiconductors, field-effect transistors (FETs), contact resistance, device reliability

# **INTRODUCTION**

Transistors, the fundamental building blocks of logic and memory technologies, must evolve continuously to achieve and sustain high performance while operating within reasonable energy budgets, especially with the emergence of performancedemanding and energy-consuming Artificial Intelligence (AI) systems. Silicon transistors, used for more than half a century, are now struggling to meet these growing requirements, necessitating new materials that can surpass silicon's limitations.

Graphene nanoribbons (GNRs) synthesized with atomic precision through bottom-up methods<sup>2</sup> offer versatile electronic properties, making them ideal for nanoelectronic devices and particularly suitable as channel materials in field-effect transistors (FETs) as alternatives to silicon. Theoretical studies predict that GNRs possess high carrier mobility similar to that of graphene and carbon nanotubes (CNTs),<sup>3,4</sup> while overcoming issues like the lack of a band gap and purity concerns, respectively. Although this high mobility has yet to be demonstrated in GNRFET devices, Terahertz Spectroscopy

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Figure 1. On-surface synthesis of 9-AGNRs. STM topographic scan (V = -1.5 V, I = 0.03 nA) (a) and Raman spectrum (b) of a 1 monolayer-coverage sample of 9-AGNRs grown on Au(111)/mica.

measurements<sup>5</sup> have revealed very high mobility in GNRs. We<sup>6,7</sup> have also demonstrated high on-state current ( $I_{ON}$ ) and high on-off current ratios ( $I_{ON}/I_{OFF}$ ) in GNRFETs.

The bottom-up synthesis of GNRs differs significantly from the top-down fabrication of silicon transistors, which involves "sculpting silicon." This bottom-up approach offers unparalleled design flexibility and atomic precision, for example, enabling the creation of GNRs with tunable band gaps through controlled edge width and topologies.<sup>8–10</sup> Such flexibility contrasts sharply with the inherent limitations of silicon technology, which lacks the ability to tune material properties to this extent.

The feasibility of fabricating GNRFETs has been demonstrated in several studies.<sup>11,12</sup> While ongoing research<sup>6,7,13–20</sup> primarily focuses on enhancing their performance, the longterm stability and reliability of GNRFETs have not yet been thoroughly investigated. Studies<sup>21–23</sup> have shown that FET devices with other low-dimensional materials tend to degrade over time, suggesting that GNRs are likely to face similar stability issues. Addressing this aspect is just as crucial as performance. Even if the desired performance is achieved, potential reliability issues could pose significant challenges for large-scale integration in practical applications.

In this work, we studied the long-term stability and reliability of the FETs made with nine-atom-wide armchair GNRs (9-AGNRFETs). We showed that the electrical performance of the 9-AGNRFETs deteriorates over consecutive logic cycles. To address this issue, inspired by previous work<sup>21–23</sup> on other low-dimensional materials where encapsulation of the devices with various dielectric materials was found to be successful in enhancing stability and reliability, we deposited a thin aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) layer directly on the GNRFETs by atomic layer deposition (ALD). We thoroughly investigated the deposition quality of the ALD Al<sub>2</sub>O<sub>3</sub> layer, its impact on the GNR structure and device characteristics, and discussed the mechanisms behind degradation and how the ALD layer enhances long-term device stability and reliability.

### **RESULTS AND DISCUSSION**

We synthesized 9-AGNRs on Au(111)/mica substrates using the 3,6-diiodo-1,1:2,1-terphenyl (DITP) precursor following the established on-surface synthesis method.<sup>24,25</sup> The growth

process involves an Ullmann-type polymerization reaction at  $T_1 = 200$  °C followed by cyclodehydrogenation (CDH) at  $T_2$ = 400 °C. Synthesis details are provided in the experimental section. A typical scanning tunneling microscope (STM) image of a 9-AGNRs sample grown on Au(111), shown in Figure 1a, reveals a uniform and densely packed arrangement with lengths averaging  $\sim 70$  nm and a width of  $\sim 0.95$  nm. Theoretical calculations predict a free-standing 9-AGNR bandgap of ~2.29 eV, while the experimental value measured with scanning tunneling spectroscopy (STS) on gold is  $\sim 1.4$  eV.<sup>26</sup> We used Raman spectroscopy to check the quality of the GNRs on a larger scale from multiple points across the sample. Figure 1b shows a typical Raman spectrum of the sample, exhibiting all characteristic peaks of 9-AGNRs including radial breathing like mode (RBLM), C-H, D, and G, with high intensity and sharpness, and thus confirming high quality of the sample.<sup>13,2</sup>

In order to fabricate 9-AGNRFET devices, we first transferred the GNRs onto a prepatterned SiO<sub>2</sub>/Si chip (as shown in Figure S1a-c), which houses over 1000 local backgated devices with an  $\sim$ 8 nm tungsten (W) gate metal capped with a ~5.5 nm hafnium oxide (HfO<sub>2</sub>) dielectric layer grown by ALD. We used a well-established polymer-free method for the transfer process.<sup>28</sup> After the transfer, we used Raman spectroscopy again to verify the structural integrity and quality of the GNRs. The typical Raman spectrum of the GNRs on the devices (shown in the top panel of Figure 3d) reveals all the characteristic peaks of the 9-AGNRs, alongside the absence of C-O and O-H peaks. These results indicate that the GNRs maintain their structural integrity after transfer, without damage or chemical modification.  $^{28-30}$  Once the successful transfer of the GNRs was confirmed, we fabricated ~15 nm thick palladium (Pd) contacts contacts to the GNRs, using standard electron beam lithography (EBL) writing, developing, electron-beam (e-beam) metal deposition, and lift-off process. Subsequently, we performed transport measurements of 9-AGNRFETs. After completing these measurements, we deposited a  $\sim 10$  nm Al<sub>2</sub>O<sub>3</sub> layer directly onto these devices by ALD using a trimethylaluminum (TMA) precursor at 150 °C under vacuum. We note that in our previous study,<sup>6</sup> we deposited a 1-1.25 nm Al<sub>2</sub>O<sub>3</sub> layer, referred to as the "nanofog" layer, on GNRs to facilitate the uniform growth of a 2.5 nm  $HfO_2$  layer. This was done for building double-gated



Figure 2. Fabrication of 9-AGNRFETs. (a) Schematic diagram of short-channel 9-AGNRFETs in a local back-gated geometry with an ultrathin  $HfO_2$  dielectric layer, Pd contacts, and a thin ALD layer of  $Al_2O_3$  atop the devices. (b) Low-magnification false-colored SEM image of a 9-AGNRFET device, with a high-magnification inset showing SEM of the Pd contacts. The raw SEM images are in Figure S1d,e.



Figure 3. ALD of  $Al_2O_3$  onto 9-AGNRFETs. AFM height profile images of a 9-AGNRFET device surface before (a), and after (b)  $Al_2O_3$  deposition (The images are taken with a 1000 nm x 1000 nm area, and the height profile bars show approximate max. values of 12 nm in (a) and 20 nm in (b), respectively.). (c) Cross-sectional TEM image of the  $Al_2O_3/9$ -AGNRs/HfO<sub>2</sub> film deposited on SiO<sub>2</sub>/Si wafer (Pt layer was deposited to facilitate imaging.). The TEM-energy-dispersive X-ray spectroscopy (EDX) elemental maps are given in Figure S3. (d) Raman spectra comparison of the device before and after  $Al_2O_3$  deposition. Al 2p and O 1s XPS regions (e) and XPS survey (f) of the device surface after  $Al_2O_3$  deposition.

GNRFETs in order to compare the electrical performance of the back gate versus the double gate. The schematic diagram and SEM images of 9-AGNRFET are shown in Figure 2a,b, respectively.

Now we present the results for  $Al_2O_3$  deposition. Figure 3a,b show the typical AFM height profile images taken from the surface of a 9-AGNRFET device before and after  $Al_2O_3$  deposition, respectively. The root-mean-square roughness  $(R_q)$  of the surface was measured to be ~0.688 nm before deposition and ~2.128 nm after deposition. A relatively small increase in surface roughness, as well as the absence of large pinholes or wells, indicates the uniform growth of  $Al_2O_3$  layer.



Figure 4. Transport measurements of 9-AGNRFETs. (a)  $I_{DS}-V_{GS}$  characteristics of a 9-AGNRFET device before and after  $Al_2O_3$  deposition.  $I_{DS}-V_{GS}$  characteristics of the devices at different cycle number before (Device 3) (b) and after (Device 2) (c)  $Al_2O_3$  deposition. The forward and reverse sweeps are averaged together. The original data is given in Figure S5. (d)  $I_{DS}-V_{DS}$  characteristics of the device in (a) after  $Al_2O_3$ deposition. (e) Reliability test results for four devices ( $I_{ON}$  vs measurements cycle number): two tested before (Device 3 and Device 4) and two after (Device 1 and Device 2)  $Al_2O_3$  deposition. All measurements were performed at  $V_{DS} = -1$  V under ambient conditions.

Two additional AFM images for each are also provided in Figure S2a,b. The cross-sectional transmission electron microscopy (TEM) image of Al<sub>2</sub>O<sub>3</sub>/9-AGNRs/HfO<sub>2</sub> film deposited on SiO<sub>2</sub>/Si wafer (Figure 3c) and EDX mapping (shown in Figure S3) further confirm the uniformity of  $Al_2O_3$ layer and absence of diffusion of Al atoms into the other layers. In addition to AFM and TEM characterization, we performed X-ray photoelectron spectroscopy (XPS) directly on the chip after deposition. Figure 3e shows the XPS spectra of the Al 2p and O 1s regions. The spectra display typical peaks at ~74.6 and ~531.5 eV for Al 2p and O 1s of Al<sub>2</sub>O<sub>3</sub>, respectively. These peaks are consistent with previous reports on Al<sub>2</sub>O<sub>3</sub>. Furthermore, the XPS survey spectra, as shown in Figure 3f, do not show any major peaks from the underlying substrate including HfO2 and W layers. Given that XPS beams can penetrate to a maximum depth of  $\sim 10$  nm, and the spot size is up to ~200  $\mu m_{i}^{32}$  the absence of these Hf and W peaks confirms that there are no large pinholes; otherwise, we would be able to see the peaks from the underlying structures. Overall, these results confirm the uniform deposition of Al<sub>2</sub>O<sub>3</sub> layer.

Due to their 1D nature and small width ( $\sim 0.95$  nm for 9-AGNR), nucleation of ALD species may initiate preferentially in-between the GNRs on the underlying HfO<sub>2</sub> dielectric layer, where the surface area is higher and the binding sites are more accessible. Once nucleation occurs at the edges, ALD species can then grow and easily cover the entire surface of the GNRs. Additionally, the small width of the GNRs minimizes the possibility of nonuniformities compared to larger surfaces. In

fact, obtaining such uniform dielectric deposition on 2D materials, such as graphene and transition metal dichalcogenides (TMDs), has been found to be quite challenging.<sup>33–35</sup> While 2D materials offer a larger surface area for nucleation compared to GNRs, their larger size and 2D structure may also lead to potential nonuniformities in coverage, especially in the presence of vacancies or defects. These vacancies/defects can act as nucleation sites, potentially leading to nonuniform nucleation and growth of ALD species. Despite these challenges, recent studies have shown that a ultrathin "nanofog" layer can facilitate highly uniform deposition of dielectrics on these materials.<sup>33,36</sup>

To check whether the GNRs are damaged during the ALD process and if there is any chemical interaction with the  $Al_2O_3$ film, we characterized the sample using Raman spectroscopy. Figure 3d shows the comparison of the typical Raman spectra of the GNRs before and after Al<sub>2</sub>O<sub>3</sub> deposition. All the characteristic GNR peaks are maintained without noticeable shift, indicating that the GNRs are not damaged or chemically modified during the ALD process. Nevertheless, the peak intensities are observed to be lower compared to before deposition. We believe that the decrease in peak intensities is not indicative of lower GNR quality, but rather originates from optical interference effects of Al<sub>2</sub>O<sub>3</sub> layer, which can alter light scattering and absorption properties, thereby affecting the Raman signal intensities.<sup>13,37</sup> If GNR quality was affected, we would observe shifts in the peaks, disappearance or broadening of the RBLM peak, which is known to be highly sensitive to

GNR quality,<sup>38</sup> and we would expect to see only a reduction in the GNR peaks, not silicon.

Figure 4a exhibits the transfer characteristics (drain current  $(I_{\rm DS})$  as a function of gate voltage  $(V_{\rm GS})$  at a constant drainsource voltage bias  $(V_{DS})$  of -1 V) of a 9-AGNRFET. The transfer characteristics of the device are shown before and after the deposition of a thin  $Al_2O_3$  layer and are representative of all GNR devices under investigation. The device exhibits a predominant p-type FET behavior with an  $I_{ON}$  above 1  $\mu$ A and an  $I_{\rm ON}/I_{\rm OFF}$  ratio of ~10<sup>3</sup>. Only a small difference is observed between the device characteristics before and after  $Al_2O_3$  where a slightly smaller  $I_{ON}$  could be explained by remote phonon scattering,<sup>39</sup> and  $I_{ON}$  could be improved by the deposition of a the top-gate metal.<sup>6</sup> Figure 4d shows the typical output characteristics ( $I_{DS}$  vs  $V_{DS}$ ) of the device after Al<sub>2</sub>O<sub>3</sub> deposition is shown, revealing a nonlinear curve indicative of Schottky barrier at the GNR-contact. The detailed statistical distribution of the key device parameters, including  $I_{ON}$ ,  $I_{OFF}$ ,  $I_{\rm ON}/I_{\rm OFF}$ , and subthreshold swing (SS) for several 9-AGNRFETs before and after Al<sub>2</sub>O<sub>3</sub> deposition is given in Figure S4. Overall, our results indicate that there is no significant chemical reaction with or fixed charge in the Al<sub>2</sub>O<sub>3</sub> immediately after deposition.

Figure 4b,c gives an overview of the evolution of the  $I_{\rm DS}-V_{\rm GS}$  characteristics of Device 3/Device 2, as they are cycled 1200 times. The original data is given in Figure S5. To evaluate the reliability of the as-fabricated 9-AGNRFETs, we performed repeated full cycles (round trip) of  $V_{\rm GS}$  from 3.5 to -3.5 V at  $V_{\rm DS} = -1$  V under ambient conditions and recorded the  $I_{\rm ON}$  values. Each cycle lasted approximately 38 s, during which 120 data points were collected. After each cycle, the devices are allowed a 30 s rest period. In Figure 4e, the results of the  $I_{\rm ON}$  from the four different devices are presented for 1200 measurement cycles: Device 3 and Device 4 before Al<sub>2</sub>O<sub>3</sub> deposition in orange and red, and Device 1 and Device 2 after Al<sub>2</sub>O<sub>3</sub> deposition. The  $I_{\rm ON}$  of the devices without Al<sub>2</sub>O<sub>3</sub> decreases significantly with the number of cycles, indicating that the devices degrade over time.

To understand the mechanism of the degradation, we note that the Al<sub>2</sub>O<sub>3</sub> deposition does not eliminate degradation mechanisms for the channel or the dielectric/channel interface. This means that a degradation of the current-voltage characteristics due to changes in the dielectric/channel interface, which is usually observed in transistors, is not an explanation for the GNRFETs considered here. We also remark that self-heating effects are not an explanation since the current density is on the order of 1  $\mu$ A, which is similar or lower than the current typically observed in silicon transistors. Calculations also show that the maximum temperature in the GNR channel will be lower than 100  $^{\circ}C$ ,<sup>40</sup> and this heat will dissipate quickly into the underlying dielectric layer. Moreover, GNRs, especially those with armchair edges, remain stable at temperatures up to 430 °C.<sup>29</sup> To further support this, we performed Raman mapping characterization (shown in Figure S6) following the reliability measurements. The results indicate no significant alterations in the Raman spectra within the device at the micrometer scale, suggesting that the GNRs remain intact and have not been severely affected. Therefore, the degradation mechanism must be sought elsewhere.

A degradation of the contact resistance is the most likely explanation for the observed degradation. For this purpose, we conducted TEM/EDX analysis (see Figure S7) on the Pd interface of a Device 3 that we measured its reliability before  $Al_2O_3$  deposition. The EDX mapping revealed a heightened oxygen concentration on the Pd surface, but we could not determine whether this oxygen originates from the surrounding dielectric or from an oxide layer formed around the Pd. The e-beam deposition of metal contacts, such as Pd, onto low-dimensional materials can result in defective, disordered, nonuniform, and/or contaminated interfaces.<sup>13,41</sup> A defective Pd surface could oxidize under the application of a voltage. Another explanation could be that the absorption of water changes the dielectric environment near the contact and increases the contact resistance.<sup>42</sup> Regardless of the precise microscopic mechanism of the contact degradation, we observe that encapsulation with  $Al_2O_3$  stops the degradation from taking place.

The results of the I<sub>ON</sub> from the two distinct GNRFET devices (Device 1 and Device 2 in green) following  $Al_2O_3$ deposition presented in Figure 4e for 1200 measurement cycles reveal consistent performance without any signs of degradation or alteration. Moreover, the data show reduced noise and enhanced stability compared to measurements taken prior to Al<sub>2</sub>O<sub>3</sub> deposition. To further validate this, we repeated the measurements for up to 8000 cycles (Figure S8), and the devices maintained their performance. We also applied the same procedure using ALD grown silicon nitride  $(SiN_r)$ , which exhibited similar stability behavior, confirming the generality of our technique (Figure S9). These results indicate that depositing dielectric layers effectively isolates the contact metal and channel surface from exposure to air, thereby reducing or fully eliminating environmental interactions such as oxidation.

### **CONCLUSIONS**

In conclusion, we comprehensively investigated the long-term stability and reliability of 9-AGNRFETs. Our results indicate that the performance of these devices degrades over time when exposed to ambient conditions during measurement cycles. We identified and thoroughly discussed the possible degradation mechanisms, primarily attributing them to the degradation of contact resistance. To address this issue, we successfully deposited a thin  $Al_2O_3$  layer directly onto the devices using ALD. We demonstrate that  $Al_2O_3$  uniformly grows on top of the GNRs without causing any damage. The  $Al_2O_3$  layer acts as an effective barrier, reducing environmental interactions and thereby extending the lifespan of the devices. We believe that our study could facilitate the large-scale integration of GNRFETs into practical applications and provide valuable insights for further performance improvements.

#### **EXPERIMENTAL SECTION**

**Growth and STM of 9-AGNRs.** Au(111)/mica substrates (Phasis, Switzerland) were cleaned in ultrahigh vacuum (UHV) with two cycles of sputtering at 1 kV Ar<sup>+</sup> for 10 min and annealing at 470 °C for 10 min. The 9-AGNR precursor monomer DITP was then sublimated onto the clean Au surface from a quartz crucible heated to 70 °C while the substrate remained at room temperature. High-coverage samples were obtained by molecule deposition for 8 min with a 1 Å per minute sublimation rate. Following deposition, the substrate was heated to 200 °C (0.5 K/s) for 10 min to initiate DITP polymerization, followed by annealing at 400 °C (0.5 K/s) for 10 min to form the GNRs by cyclodehydrogenation. STM images of 9-AGNRs grown on Au(111)/mica were acquired at room temperature using a Scienta Omicron VT-STM. Topographic images were acquired in constant current mode using a sample bias of -1.5 V and a set point current of 0.03 nA.

Transfer of 9-AGNRs. The as-grown GNRs on the Au substrate were first transferred onto prepatterned local back-gated chips. The fabrication details of the chips are given in the subsequent sections. The transfer process was carried out using the polymer-free method reported in our previous work.<sup>43</sup> First, the GNRs/Au(111)/mica substrate were floated in 37% HCl. This caused the mica to delaminate and sink, leaving the GNRs/Au(111) film floating on the HCl surface. Next, the GNR/Au(111) film was lifted from HCl with the chip, resulting in GNRs between the chip surface and Au(111)film. To increase adhesion, a drop of isopropanol was placed on the Au(111) film, followed by annealing on a hot plate for 10 min at 80 °C. After annealing, the Au(111)/GNR/chip was first covered with 2 to 3 drops of potassium iodide  $(KI_2)$  gold etchant, then submerged in KI<sub>2</sub> for 5 min. Finally, the GNR/chip sample was cleaned by submersion in DI water for 5 min, then rinsed with isopropanol and dried under a nitrogen stream.<sup>6</sup>

ALD of Al<sub>2</sub>O<sub>3</sub> onto 9-AGNRFETs. We deposited ~10 nm Al<sub>2</sub>O<sub>3</sub> layer using the Fiji ALD system directly onto the GNRFETs using TMA precursor at 150 °C under vacuum. The film's thickness was verified by ellipsometry using the J.A. Woollam Ellipsometer.

**ALD of SiN<sub>x</sub> on 9-AGNRFETs.** SiN<sub>x</sub> was deposited on 9-AGNRFETs using using the Fiji ALD system. Bis(tertiarybutylamino) silane (BTBAS) and nitrogen (N<sub>2</sub>) plasma were used as the Si and N<sub>2</sub> sources, respectively. The substrate temperature was maintained at 200 °C, and N<sub>2</sub> plasma was pulsed for 1 s during each cycle. A total of 300 cycles were completed, and the devices were measured directly without any further processing. The more details of the deposition can be found in a previous study.<sup>44</sup>

**Raman Spectroscopy.** We used a Renishaw Raman microscope with a 785 nm laser, keeping the power under 10 mW, and a  $50\times$  objective lens. We collected at least ten spectra from different points for each sample. The background of the Raman spectra for the GNRs on Au was subtracted.

**XPS of Al**<sub>2</sub>**O**<sub>3</sub>. Surface chemical analysis of the Al<sub>2</sub>O<sub>3</sub> layer was performed using a Kratos Axis Ultra 165 photoelectron spectrometer with base pressure at  $1 \times 10^{-8}$  Torr, equipped with a monochromatic Al K $\alpha$  X-ray source at 20 mA/15 keV.

**AFM.** AFM height profile images were captured using a Park AFM system under ambient conditions to determine surface roughness values prior to and following transfer, as well as after  $Al_2O_3$  deposition.

**Preparation of Pre-Patterned Local Bottom Gate Chips.** The base substrate consists of 100 nm SiO<sub>2</sub>/Si. The local back gates consist of ~8 nm of W, deposited through sputtering, then patterned using photolithography and wet etched with hydrogen peroxide  $(H_2O_2)$ . The ~5.5 nm thick HfO<sub>2</sub> layer was grown by ALD using Tetrakis(dimethylamino)hafnium (C<sub>8</sub>H<sub>24</sub>HfN<sub>4</sub>) precursor at 135 °C. Alignment markers and large electrical probing pads were patterned using standard photolithography and a lift-off process involving ~3 nm of Chromium (Cr) and ~25 nm of Platinum (Pt). The wafer was then diced into several individual chips, each measuring 1 cm by 1 cm and containing over 250 local back gated devices.

**Fabrication of Metal Contacts.** The process for patterning Pd contacts to the GNRs began with spin coating the prepatterned chip with poly(methyl methacrylate) (PMMA) n950k A2 resist at 4500 rpm, followed by a bake at 180 °C for 10 min. The EBL process was then employed using an Elionix ELS-7000 100 kV EBL system to precisely align on the prepatterned chip and expose the electrode locations. Subsequently, the chip underwent development by immersion in a chilled 3:1 IPA-MIBK solution for 90 s. Deposition of ~15 nm of Pd onto the chip was achieved using an Edwards Auto 306 e-beam deposition system operating at a pressure of ~10<sup>5</sup> Torr. Finally, the chip was immersed in Remover PG at ~65 °C to complete the lift-off process.

**SEM.** The devices were imaged using a Mira3 Tescan SEM with a 10–15 kV accelerating voltage, using secondary electrons.

**Transport Measurements.** The electrical transport measurements were performed using a Lakeshore TTPX cryogenic probe station, in conjunction with M81-SSM synchronous source measure

system and MeasureLINK software. All measurements were conducted under ambient conditions unless specified.

**FIB/TEM.** The FEI Helios DualBeam SEM/FIB equipped with an Elstar electron gun and monochromator and Tomahawk  $Ga^+$  ion column was used to create the sample section. A Pt coating layer was deposited at the surface of the sample to protect the surface of the sample during the FIB sample extraction. The Hitachi HF5000, with an accelerating voltage of 200 kV, was used to obtain TEM images and EDX for the cross-section of the sample.

## ASSOCIATED CONTENT

#### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c04097.

Optical microscopy images of chips with 9-AGNRFET devices at various magnifications; raw SEM images of 9-AGNRFETs; AFM characterization of device surfaces before and after  $Al_2O_3$  deposition; TEM cross-section and EDX mapping of  $Al_2O_3/9$ -AGNRs/HfO<sub>2</sub>film on SiO<sub>2</sub>/Si wafer; additional transport characteristics before and after  $Al_2O_3$  deposition, including CDF of  $I_{ON}$ ,  $I_{OFF}$ ,  $I_{ON}/I_{OFF}$ , and SS; reliability measurements up to 8000 cycles; Raman mapping of C–H, D, and G modes after reliability measurements; postreliability TEM and EDX; reliability measurements with SiN<sub>x</sub>, including Raman spectra and XPS survey (PDF)

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#### Author Contributions

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#### Notes

The authors declare no competing financial interest.

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